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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,519	08/18/2003	Naoki Kuwata	122.1561	1583

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EXAMINER	
JOSEPH, JAISON	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/642,519	KUWATA ET AL.	
	Examiner	Art Unit	
	JAISON JOSEPH	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 8-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-10* is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 11/21/2008 toward claim 4 have been fully considered but they are not persuasive.

Regarding claim 4, Applicant argues, *"Claim 4 was rejected under 35 U.S.C. § 102(a) as anticipated by the section of the subject application entitled "Background Art," to which the Office Action refers as "APAA." The rejection is traversed. Reconsideration is earnestly solicited."* However Examiner respectfully disagrees. Examiner relied upon the rejection is the sections of specification applicant admitted as prior art. What described in the "background art" is prior art as applicant admitted in the specification (see page 12 brief description of drawings). Further applicant disclose in the specification that "Figure 1 is a diagram showing configuration examples of high-speed optical communication systems according to the prior art." (See page 2 lines 10 -13). Further figures 2 – 5 are describing the prior art in detail. Therefore figures 2 – 5 are also prior art. Therefore the claim rejection of claim 4 based on the background art is proper. Therefore Examiner maintains the rejection of claim 4.

Applicant further argues *"The second clause of claim 4 recites:*

Wherein said phase comparator circuit comprises two phase comparator circuits.

The section of the subject application entitled Background Art neither teaches, discloses, nor suggests "wherein said phase comparator circuit comprises two phase comparator circuits," as recited in claim 4. The EXORs 45 and 46 shown in Fig. 3 of the

subject application, rather, to which the Office Action analogizes the recited "two phase comparator circuits," are part of a single phase comparator circuit.

However Examiner respectfully disagrees. The limitation recites as applicant admitted "the phase comparison circuit comprises two phase comparison circuits". It is well known in the art that EXOR circuit is used as a phase comparator. Therefore EXOR 45 and 46 are the two phase comparison circuits in the phase comparison circuit.

Applicant further argue, *"The section of the subject application entitled Background Art neither teaches, discloses, nor suggests two phase comparator circuits "which perform phase comparison at every other bit of said data signals and respectively accept phases differing by one cycle (1/B sec) of said data signal to perform phase comparisons for all data signals," as recited in claim 4. Claim 4 is submitted to be allowable. Withdrawal of the rejection of claim 4 is earnestly solicited."* However Examiner respectfully disagrees. In figure 3 of the applicant admitted prior art teaches "the oscillation center frequency of the VCO 50 is equal to one half the bit rate of the received data signal (1)" (see page 6, lines 9 – 11 of the specification). Which indicate the data can only detected on every other bit since the frequency of the clock signal is one half of the data rate. AAPA further teach "[t]he received data signal (1) is input to two D-flip/flops 51 and 52, which correspond to the discrimination circuits 37 and 38 in part (b) of FIG. 1, and signals (3) and (4) ***respectively synchronized to the falling and rising edge signals*** from the PLL circuit" (see page 6, lines 11 – 16 of the specification). Flip-flop 51 and 52 re synchronized to falling and rising edge of the clock signal respectively. Flip-flop 51 latch data on the falling edge of the clock and flip-flop 52

latch data on the rising edge of the clock. since the input data have a data rate of two times of the clock frequency, using two flip-flop, one latch data on the rising edge and the another one latch data on the falling edge of the clock, all the data can be recovered. A flip flop can latch data using only a rising edge or falling edge of the clock signal. Therefore the data rate if the input signal is twice the clock frequency, only every other bit of the data steam can be latched. Since one of the flip flop latch data on the rising edge and the other one latch data on the falling edge of the clock signal, all the data can be recovered which is equivalent of having a clock frequency same as the data rate. Thus flip-flop 51 and 52 are latching only every other bit of the data steam. Output of flip-flop 51 is inputted into the phase comparator 46 and the output of the flip-flop 52 is inputted to phase comparator 45. Thus phase comparator 45 and 46 are performing a phase comparison at every other bit of said data signals and respectively accept phases differing by one cycle (1/B sec) of said data signal to perform phase comparisons for all data signals. Thus Applicant Admitted Prior Art teaches all cited limitations. Therefore Examiner maintains the rejection of claim 4.

Applicant's arguments with respect to claims 1 – 3 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1 – 3 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1, recite the limitation, "... a control circuit controlling, upon detecting said absence, the phase of said clock signal by a change of the phase in order to maintain synchronization ***by using phase information on a data signal which is not used by said phase comparator circuit before detecting said absence***" which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Figure 10 disclose the control circuit is controlling the phase lock signal based on the output of both phase comparators 45 and 46. thus the claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. For the purpose of the art rejection, Examiner consider the claims without the limitation "…by using phase information on a data signal which is not used by said phase comparator circuit before detecting said absence…".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim 4 is rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (AAPA).

Regarding claim 4, AAPA discloses a timing extraction circuit which uses a PLL circuit containing a phase comparator circuit for performing a phase comparison between a data signal of bit rate B ad a clock signal of B/2 at intervals of 2/B (see figure 3 components 45, 46 page 4, line 11 – page 5, line 4 of the present specification) AAPA further discloses said phase comparator circuit comprises two phase comparator circuits which perform comparison at every other bit of said data signals and respectively accepts phases differing by one cycle of said data signal to perform comparisons for all data signals (see figure 3, components 45, 46 and page 4, line 11 – page 5, line 4 of the present specification, it is inherent that the each of the phase comparator circuits do the comparison at every other bit f said data signal since the figure 3 shows a half frequency clock extraction method. Half frequency extraction method uses a clock that is half the frequency of the data signal. Thus it can only compare every other bit of the received data.)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims1 – 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Soda (US Patent 5,956,378).

Regarding claim 1, AAPA discloses a timing extraction circuit which uses a PLL circuit containing a phase comparator circuit for performing a phase comparison between a data signal of bit rate B ad a clock signal of B/2 at intervals of 2/B (see figure 3), AAPA does not disclose the timing extraction circuit further comprise a detection circuit for detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of prescribed pattern; and a control circuit for controlling upon detecting said absence, the phase of said clock signal in order to maintain synchronization.

In analogous art, Soda teaches a PLL circuit comprising a detection circuit for detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of prescribed pattern before the occurrence of a loss of synchronization at the Phase locked loop (see figure 2, component 23 and column 4, line 14 – 33); and a control circuit for controlling upon detecting said absence, the phase of said clock signal in order to maintain synchronization (see figure 2, component 23 and column 4, line 14 – 33) [Applicant admits that when the PLL circuit

receives a prescribed pattern, the PLL will run out of synchronization (i.e. if the prescribed pattern is detected (absence of the comparison output), it will indicate the possible collapse of the synchronization). Soda teaches a detector detecting the collapse of the synchronization from the output of the phase comparator is equivalent to detecting the prescribed pattern (absence of the comparison output).].). Therefore it would be obvious to an ordinary skilled in the art at the time the invention was made to incorporate the Soda's PLL control circuit in AAPA to have a phase locking loop circuit which need not have an adjusting terminal for use in adjusting the frequency range.

Regarding claim 2, which inherits the limitations of claim 1, Soda further teaches control circuit controls the phase of said clock signal by inverting said clock signal (see column 6, lines 15 –39).

Regarding claim 3, which inherits the limitation of claim 1, Soda further teaches said control circuit controls the phase of said clock signal by controlling a VCO.

Allowable Subject Matter

Claims 8 – 10 are allowable over prior art of record.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAISON JOSEPH whose telephone number is (571)272-6041. The examiner can normally be reached on M-F 9:30 - 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. J./
Examiner, Art Unit 2611

/Chieh M Fan/
Supervisory Patent Examiner, Art Unit 2611